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HP 12968A ASYNCHRONOUS COMMUNICATIONS INTERFACE DIAGNOSTIC

reference manual

For hp- 2100 Series Computers

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MICROFICHE PART NO. 12968-90004

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic confirms proper operation of the HP 12968A Asynchronous Communications Interface. The basic I/O portion of the interface, which includes the Flag and Control circuits, will be tested. The status, control, receive, and transmit features will also be tested. The interface will be used with skip on flag, interrupt, and Dual-Channel Port Controller (DCPC)*. This test uses a test hood along with special status bits provided for self testing.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. An HP 2100 Series Computer with a minimum 4K memory.

b. An HP 12968A Asynchronous Communications Interface Kit with hooded self-test connector, Part No. 12966-60003 (the self-test connector wiring is shown in figure 1-1).

c. A teleprinter (console device) for message reporting (recommended but not required).

d. A loading device for loading the diagnostic program.

1-3. SOFTWARE REQUIREMENTS

The following software is required:

a. Diagnostic Configurator (part numbers below) is used for equipment configuration and as a console device driver.

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

b. HP 12968A Asynchrounous Communications Interface (hereafter called Async Comm Intfc) Diagnostic binary object tape Part No. 12968-16001.

The diagnostic serial number (DSN) is contained in memory location 126 (octal) of the program. The DSN for this diagnostic is 103121 (octal).

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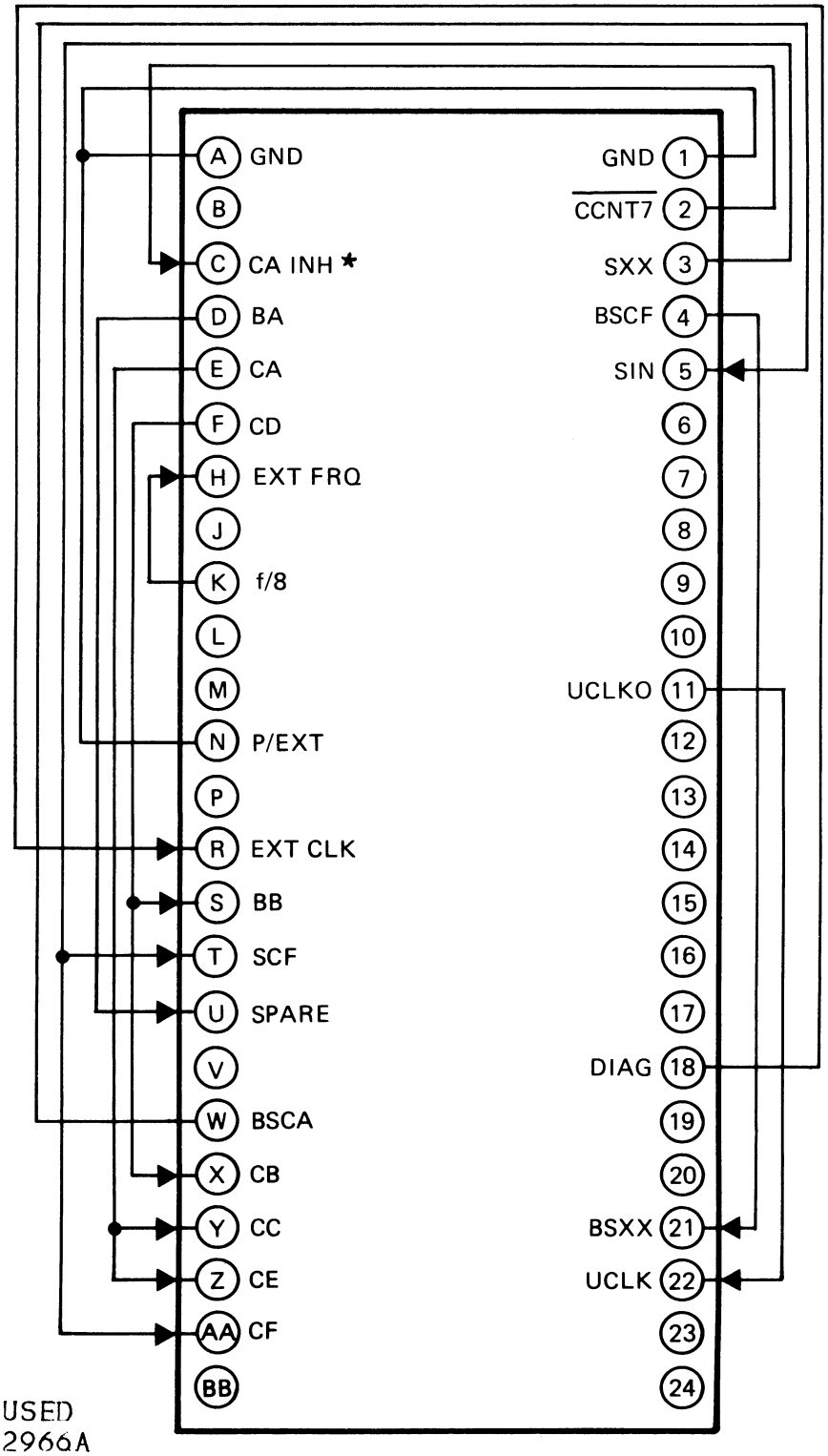
*Or Direct Memory Access (DMA).



* CA INH USED ON HP 12966A ONLY.

Figure 1-1. Test Connector (12966-60003)

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program consists of 11 tests plus a Control and Initialization section. The Control and Initialization section accepts the select code and options required by the tests. The tests are called into execution by the Control section as sequential or selectable subroutines. The following functions are placed under test by this diagnostic:

Flag and Control (Basic I/O) - (TSTØØ)
Master Reset Command - (TSTØ1)
Modem related signals - (TSTØ2)
Reference and Enable Commands - (TSTØ3)
Character Counter - (TSTØ4)
Transmit operation - (TSTØ5)
Receive operation - (TSTØ6)
Baud rate selection - (TSTØ7)
Parity Error and Overrun - (TST1Ø)
DCPC related circuits and data transfer - (TST11)

2-2. TEST CONTROL AND EXECUTION

The diagnostic outputs a title message to the console device (if present) for operator information, then executes the tests according to the options selected on the Switch Register. The Control section primarily checks Switch Register bits 15, 13 and 12.

The Control section also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 1Ø is clear). The count will be reset only if the diagnostic is restarted.

Test sections are executed one after the other in each diagnostic pass. User selection or default will determine which test sections will be executed. Switch Register bit 9 is used to indicate that test selection is desired. (Refer to paragraph 3-4.)

2-3. MESSAGE REPORTING

There are two types of messages, error and information. Error messages are used to inform the operator of a failure of the interface to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform an operation related to a function of the unit. In the latter case an associated halt will occur to allow the operator time to perform the function. The operator must then press RUN.

If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available.

Example - Error with halt

Message: E016 CLC SC (Console Device)
Halt Code: 102016 (T- or Memory Data Register)

Example - Information with halt

Message: H024 PRESET RUN
Halt Code: 102024

Example - Information only

Message: H025 BI-0 COMP
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by setting Switch Register bit 10. Operator intervention is suppressed by setting Switch Register bit 8 (i.e. BI-0). When Switch Register bit 12 is set the tests that are selected will be repeated and all operator intervention will be suppressed.

2-4. DIAGNOSTIC LIMITATIONS

2-5. PRIORITY STRING

The interface's capability of receiving, passing and denying priority is not completely checked by this diagnostic. If the interface does not receive priority, (PRH from the next lower select code) an error E014 NO INT will occur. To check this remove an interface of a lower select code and run the Basic I/O test and the above mentioned error should occur. Checking the interface's ability to pass or deny priority is beyond the scope of this diagnostic.

2-6. LOGIC ELEMENT

The SRB/BSRB Line Receiver circuit is not placed under test by this diagnostic.

2-7. ELECTRONIC COMPONENTS

The TTY IN and XMIT I circuits are not placed under test by this diagnostic.

Section III

OPERATING PROCEDURES

3-1. OPERATING PROCEDURES

A flowchart for loading this diagnostic in conjunction with the Diagnostic Configurator is provided in figure 3-1.

If an unconfigured Diagnostic Configurator is to be used start at entry point A.

If a configured Diagnostic Configurator is to be used start at entry point B.

If a combined configured Diagnostic Configurator and an unconfigured Diagnostic is to be used start at entry point C.

If a combined configured Diagnostic Configurator and a configurated Diagnostic is to be used start at entry point D.

Note: Before the Async Comm Intfc Diagnostic is executed, the test hood must be installed.

3-2. RUNNING THE DIAGNOSTIC

The program will execute the diagnostic according to options selected in the Switch Register. At the completion of each pass of the diagnostic, the pass count is printed on the console device. If Switch Register Bit 12 was not set, the computer will halt with 102077 in the Memory Data (T-) Register. At this point the A-register contains the pass count. To run another pass, the operator need only press RUN.

3-3. RESTARTING

The program may be restarted by setting the P-register to 2000 (octal). Select Switch Register options shown in table 3-2 and press RUN.

If a trap cell halt occurs (106077), the operator must determine the cause of either the interrupt or the transfer of control to the location shown in the M-register. The diagnostic may have to be reloaded to continue.

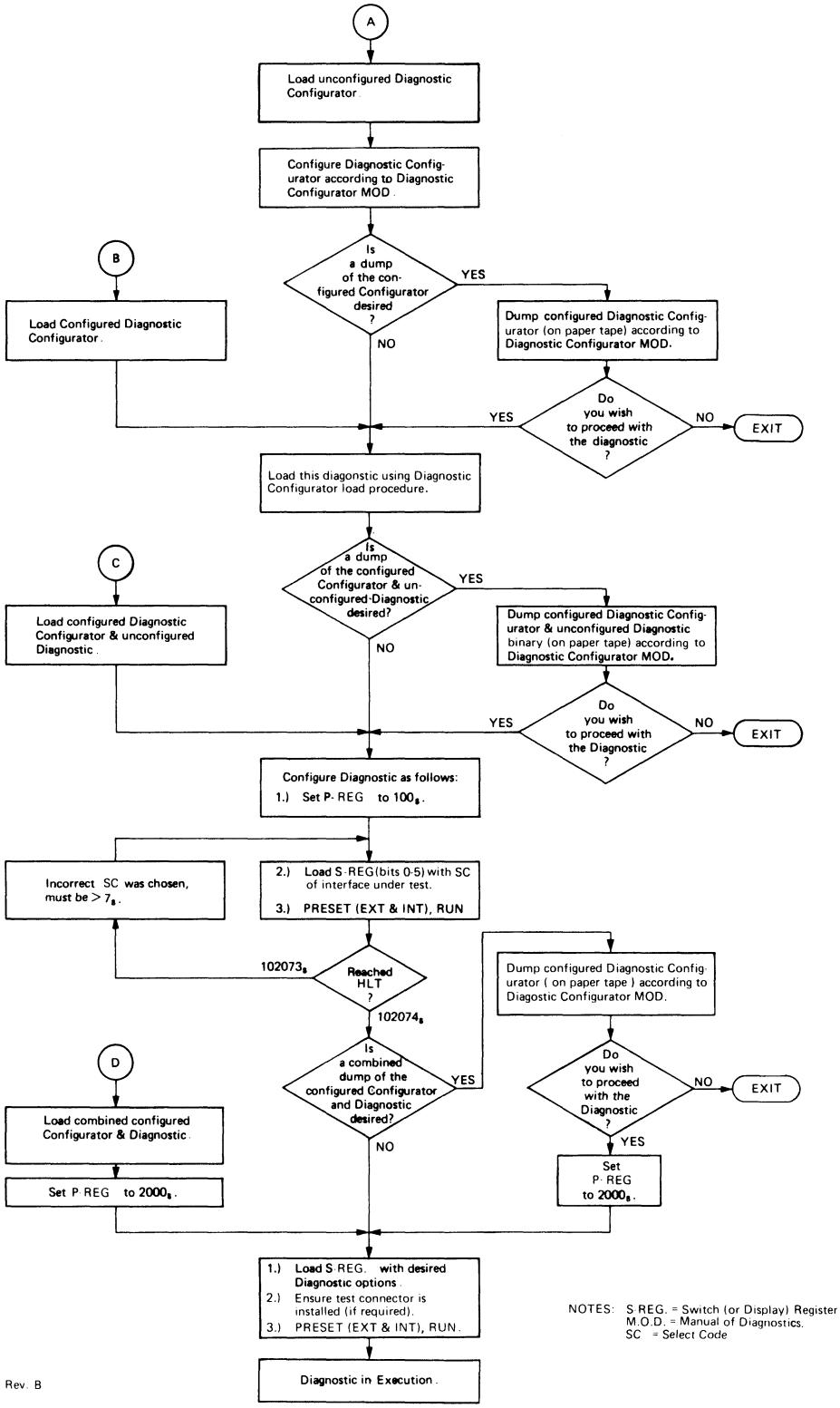


Figure 3-1. Load/Start Procedure Flowchart

3-4. TEST SELECTION

The Control section of the diagnostic provides the operator with a method to select his own test, or sequence of tests, to be run. The operator sets Switch Register bit 9 to indicate the desire to make a selection. The computer will come to a halt 102075 to indicate it is ready for selection. If the program is running, the current test will be completed then the halt will occur. The operator then loads the A-Register with the tests desired. A-register bit 0 represents Test 00, bit 1 represents Test 01, and so on through bit 9 which represents Test 11 (see table 3-1). The operator must then clear Switch Register bit 9 and press RUN. The selections will then be run. If all bits are cleared the standard sequence will be run.

Table 3-1. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	Test 00
1	Test 01
2	Test 02
3	Test 03
4	Test 04
5	Test 05
6	Test 06
7	Test 07
8	Test 10
9	Test 11
10-15	Reserved
B-Register	Reserved

Table 3-2. Switch Register Options

BIT	MEANING IF SET
Ø	Reserved
1	Reserved
2	Report all errors if set. If clear, suppress excessive error reports.
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (1Ø2Ø75); operator may specify a new group of tests in the A-register, clear bit 9 of the Switch Register and press RUN.
1Ø	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 1Ø is set or console device is not present. Also, those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (1Ø2Ø76) at the end of each test; the A-register will contain the test number in octal.

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Figure 4-1 (at the end of this section) illustrates the command formats and the interface status word. Refer to table 4-2 for additional details on the content of each test.

4-2. BASIC I/O TEST ØØ

Subtest 1 - Checks the ability to clear, set and test the interrupt system. The following instruction combinations are tested:

CLF Ø - SFC Ø
CLF Ø - SFS Ø
STF Ø - SFC Ø
STF Ø - SFS Ø

Errors in the above sequences produce error messages EØØØ through EØØ3 as shown in table 4-2.

Subtest 2 - Checks the ability to clear, set and test the interface Flag. The following instruction combinations are tested:

CLF SC - SFC SC
CLF SC - SFS SC
STF SC - SFC SC
STF SC - SFS SC

Errors in the above sequences produce error messages EØØ5 through EØ1Ø as shown in table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the Flag and Control set on the interface and the interrupt system off. The sequence of instructions is shown below:

STF Ø
STF SC
STC SC
CLF Ø

The CLF Ø instruction should inhibit an interrupt from occurring from the interface. Error message EØØ4 occurs if CLF Ø fails.

Subtest 4 - Checks that the Flag of the interface under test is not set when all other select code Flags are set. Error message E011 occurs if a Flag is set incorrectly.

Subtest 5 - Checks the ability of the interface to interrupt. With the Flag and Control set and the interrupt system on, there should be an interrupt from the select code. If not, error message E014 occurs.

Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority affecting instructions is executed. The following instructions are used to check the hold-off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and/or E015 will occur if the hold-off fails. This test also checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if an interrupt does occur.

Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the SC Control and Flag set, there is no interrupt following a CLC SC instruction. The following sequence of instructions is used:

```
STC SC
STF SC
STF 0
CLC SC
```

If the CLC SC fails to inhibit an interrupt, error message E016 will occur.

Subtest 7 - Checks that the CLC Ø instruction inhibits interrupts when the SC Control and Flag are set. The following sequence of instructions is used:

```
CLF SC
STC SC
STF SC
STF Ø
CLC Ø
```

If the CLC Ø fails to inhibit an interrupt, error message EØ17 will occur.

Subtest 8 - Checks that the PRESET (EXTERNAL and INTERNAL, if applicable) switch(es) on the operator panel perform the following actions. Error messages EØ2Ø through EØ23 can occur.

Sets the interface Flag (EXTERNAL).

Clears the interface Control (EXTERNAL).

Turns off the interrupt system (INTERNAL).

Clears the I/O data lines (EXTERNAL).

4-3. MASTER RESET TEST Ø1

This test provides additional testing of the I/O portion of the interface. The operation on the CLC Ø instruction and the Master Reset Command are verified. Messages EØ3Ø through EØ34 can occur.

4-4. MODEM STATUS TEST Ø2

The test verifies the operation of the three modem control signals (CA, CD and SBA) and the five modem status lines (SBB, CB, CC, CE, and CF). Messages EØ35 through EØ42 can occur.

4-5. REFERENCE AND ENABLE COMMANDS TEST Ø3

This test verifies the operation of both the Reference and Enable Commands. Also included in this test is the Device Interrupt status bit. Messages EØ43 through EØoØ can occur.

4-6. CHARACTER COUNTER TEST Ø4

This test verifies the increment and decrement abilities of the Character Counter. Included in this test is testing of the Buffer Full and Buffer Empty Flags. Messages EØol through EØ67 can occur.

4-7. UART* TRANSMIT TEST Ø5

This test provides testing of the UART. The idle state of the BA line is examined. The start and stop bits are expected with each character transmitted. All combinations of data characters, character size, parity, and number of stop bits are tested. When error E1Ø3 occurs the actual and expected data displayed contains the start bit, the data bits, the parity bit (if used) and the stop bit(s). Messages E1ØØ through E1Ø2 can also occur.

4-8. UART RECEIVE TEST Ø6

The ability of the UART to receive data in all combinations of data format is checked. The BREAK Flag is tested. The ECHO mode of operation is included in this test. When error E1Ø5 occurs the actual and expected data are the ASCII characters and no parity, start, or stop bits are displayed. Messages E1Ø6 through E112 can also occur.

4-9. BAUD RATE SELECT TEST Ø7

This test makes a check on the ability to select (by program control) a given baud rate. A coarse check is made of the clock rate. Messages E113 through E114 can occur.

4-1Ø. OVER-RUN AND PARITY ERROR TEST 1Ø

Over-run and parity errors are generated by the program and the OVPEFLG is expected. The OVPEFLG is reset using a WORD 5 Command. Messages E115 through E121 can occur.

4-11. DCPC TEST 11

Basic DCPC control circuits ,including SRQ, are checked. If the system does not have a DCPC no data transfer will take place. With DCPC installed and configured into the Diagnostic Configurator, the program will perform testing of transmit and receive operations. Error messages E122 through E125 and E127 through E132 can occur. Information message H126 will occur if no DCPC exists.

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* See definitions of terms, paragraph 4-13.

4-12. ERROR INFORMATION MESSAGES/HALT CODES

Table 4-1 summarizes the halt codes. Table 4-2 provides a complete description of the individual halts.

Table 4-1. Halt Code Summary

HALT	MEANING
TESTS Ø to 11	
102000-102067	Error (E) and information (H) messages E000 through E067.
106000-106032	Error (E) and information (H) messages E100 through E132
CONTROL	
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of test (A-register = test number).
102077	End of diagnostic run.
106077	Trap cell halts in locations 2 though 77.

Note: See table 4-2 for a complete explanation of individual halts.

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
None	Test Control	ASYNC COMM INTFC DIAG	Header message. Output at initial start of diagnostic.
None	Test Control	Test XX	Information message before error messages (XX = test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102000	Test 0	E000 CLF 0-SFC 0	CLF/SFC 0 combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102001	Test 0	E001 CLF 0-SFS 0	CLF/SFS 0 combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102002	Test 0	E002 STF 0-SFC 0	STF/SFC 0 combination failed. STF did not set Flag or SFC caused skip with Flag set.
102003	Test 0	E003 STF 0-SFS 0	STF/SFS 0 combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102004	Test 0	E004 CLF 0 DID NOT INHIBIT INT	With interface Flag and Control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLF SC-SFC SC	CLF/SFC SC combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102006	Test 0	E006 CLF SC-SFS SC	CLF/SFS SC combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102007	Test 0	E007 STF SC-SFC SC	STF/SFC SC combination failed. STF did not set Flag or SFC caused skip with Flag set.
102010	Test 0	E010 STF SC-SFS SC	STF/SFS SC combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register contains XX, where XX = select code that caused that interface Flag to set.
102012	Test 0	E012 INT DUR-ING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupted a second time after initial interrupt was processed and interrupt system was turned back on.
102014	Test 0	E014 NO INT	No interrupt occurred with interface Flag and Control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR	Interrupt did not store the correct return address in memory.
102016	Test 0	E016 CLC SC	CLC SC did not clear interface Control with the interupt system on.
102017	Test 0	E017 CLC 0	CLC 0 did not clear interface Control.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the interface Flag.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear Control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines. Data lines should be zero.
102024	Test 0	H024 PRESET RUN	Press PRESET (EXTERNAL, INTERNAL) then RUN.
None	Test 0	H025 BI-O COMP	Basic I/O tests completed.
102026	Test 0	E026 INT EXECUTION	Interrupt was not processed correctly and one, or several, instructions were processed incorrectly during the interrupt.
102030	Test 1	E030 FLAG NOT SET - CLC 0	The Flag is reset by the program, then the instruction CLC 0 is executed. The interface Flag should be set.
102031	Test 1	E031 CONTROL NOT RESET BY CLC 0	The Control is set by the program, then the instruction CLC 0 is executed. The interface Control should be reset.
102032	Test 1	E032 FLAG NOT SET - MR	The Flag is reset by the program and a Master Reset Command is given. The Flag should be set.
102033	Test 1	E033 FLAG SET - STATUS RESET FAILED	A WORD 5 Command with a Master Reset Command is given to the interface. This command resets the status word and initializes the interface. No condition should be present that would set the Flag FF.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102034	Test 1	E034 CONTROL NOT RESET BY MR	The Control is set by the program and the Master Reset Command is sent to the interface. The Control is reset by this command.
102035	Test 2	E035 STATUS IS XXXXXX EXP YYYYYY (SBA-SCA, SBB-SCF, CF)	Using a WORD 4 Command to activate then deactivate the SBA/SCA signal, the program verifies the SBA/SCA and SBB/SCF circuits. The SBB/SCF is observed in the status word.
102036	Test 2	E036 STATUS IS XXXXXX EXP YYYYYY (CA, CC, CE)	The CA signal is activated and deactivated using a WORD 4 Command. The program observes the CC and CE bits in the status word.
102037	Test 2	E037 STATUS IS XXXXXX EXP YYYYYY (CD, CB)	The CD signal is activated and deactivated using a WORD 4 Command. The program observes the CB bit in the status word.
102040	Test 2	E040 STATUS NOT RCVD AFTER CLC SC	A known status response is expected on input after a AFTER CLC SC instruction has cleared the Control FF.
102041	Test 2	E041 STATUS RCVD AFTER STC SC	The program is not expecting to receive status on input after the STC SC instruction.
102042	Test 2	E042 STATUS IS XXXXXX EXP YYYYYY (MR)	The status is obtained following a Master Reset Command and verified.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102043	Test 3	E043 STATUS IS XXXXXX EXP YYYYYY (EN SBB-SCF)	The modem status line SBB/SCF is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102044	Test 3	E044 STATUS IS XXXXXX EXP YYYYYY (EN CF)	The modem status line CF is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102045	Test 3	E045 STATUS IS XXXXXX EXP YYYYYY (EN CE)	The modem status line CE is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102046	Test 3	E046 STATUS IS XXXXXX EXP YYYYYY (EN CC)	The modem status line CC is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102047	Test 3	E047 STATUS IS XXXXXX EXP YYYYYY (EN CB)	The modem status line CB is activated. A WORD 1 Command with the corresponding bit set is given. The status input should indicate Device Interrupt.
102050	Test 3	E050 STATUS IS XXXXXX EXP YYYYYY (REF SBB-SCF)	The modem status bit SBB/SCF is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one, then zero. The modem status bit SBB/SCF is deactivated and the WORD 2 Command testing repeated.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102051	Test 3	E051 STATUS IS XXXXXX EXP YYYYYY (REF CF)	The modem status bit CF is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CF is deactivated and the WORD 2 Command testing repeated.
102052	Test 3	E052 STATUS IS XXXXXX EXP YYYYYY (REF CE)	The modem status bit CE is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CE is deactivated and the WORD 2 Command testing repeated.
102053	Test 3	E053 STATUS IS XXXXXX EXP YYYYYY (REF CC)	The modem satus bit CC is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CC is deactivated and the WORD 2 Command testing repeated.
102054	Test 3	E054 STATUS IS XXXXXX EXP YYYYYY (REF CB)	The modem status bit CB is activated. A WORD 2 Command is given with the corresponding REFERENCE bit equal to one then zero. The modem status bit CB is deactivated and the WORD 2 Command testing repeated.
102055	Test 3	E055 STATUS IS XXXXXX EXP YYYYYY (EN MR)	The ENABLE is initialized to enable all modem status interrupts. The resetting of ENABLE by a Master Reset Command prevents the Device Interrupt from occurring.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102056	Test 3	E056 STATUS IS XXXXXX EXP YYYYYY (REF MR)	The REFERENCE is initialized to contain ones. The resetting of REFERENCE by a Master Reset Command prevents the Device Interrupt from occurring.
102057	Test 3	E057 FLAG SET - LOCK	Master Reset Command sets the LOCK. A Device Interrupt is then generated, which is prevented from setting the Flag by the LOCK.
102060	Test 3	E060 FLAG NOT SET - DEVINT	A Device Interrupt is permitted to set the Flag because the LOCK is reset.
102061	Test 4	E061 STATUS IS XXXXXX EXP YYYYYY (BFFLG)	The interface is operated in transmit mode and the UART is filled by outputting 2 characters. The Buffer Full Flag should set.
102062	Test 4	E062 FLAG NOT SET - BFFLG	A Buffer Full Flag is present and the interface should set its Flag.
102063	Test 4	E063 STATUS IS XXXXXX EXP YYYYYY (CBF)	A WORD 4 Command is given to reset the Buffer Full Flag.
102064	Test 4	E064 STATUS IS XXXXXX EXP YYYYYY (BEFLG)	The interface is placed in receive mode and characters are input, emptying the UART. The Buffer Empty Flag should set.
102065	Test 4	E065 FLAG NOT SET - BEFLG	The interface Flag should be set by the Buffer Empty Flag.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
102066	Test 4	E066 STATUS IS XXXXXX EXP YYYYYY (CBE)	A WORD 4 Command is given to reset the Buffer Empty Flag.
102067	Test 4	E067 STATUS IS XXXXXX EXP YYYYYY (CHAR CTR - MR)	The transmit Character Counter is initialized to a logical one. A Master Reset Command is then given to reset the counter.
102073	Config-uration	None	I/O select code entered at configuration is invalid. Must be greater than 7. Re-enter a valid select code and press RUN.
102074	Config-uration	None	Select code entered during configuration is valid. Enter program option bits in Switch Register and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter the desired group of tests to be executed in the A-Register, clear bit 9 of the Switch Register, then press RUN.
102076	Test Control	None	End-of-test halt resulting from Switch Register bit 15 being set (A-register equals the test number). To continue press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. Switch Register options may be changed (A-register has the pass count). To continue press RUN.
106000	Test 5	E100 BA = 0 (MR)	A Master Reset Command is given. The UART should place a logical one on line BA.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106001	Test 5	E101 DATA IS XXXXXX EXP YYYYYY (XMIT CHAR CTR)	Data is placed in the UART. The program supplies clocks using WORD 2 Commands. The program checks the contents of the Transmit Character Counter.
106002	Test 5	E102 BA = 1 (NO START)	During a transmit operation the expected start bit was not present.
106003	Test 5	E103 DATA IS XXXXXX EXP YYYYYY (UART XMIT # STOP, ZZZ PARITY, # BITS PER CHAR)	A transmit operation is performed. All combinations of data, parity, character length and no. of stop bits are used. When no teleprinter is available the A-register contains the actual data, B-register holds the expected data. The operator presses RUN and a second halt occurs (103003) with A-register holding the WORD 3 Command used to select the frame parameters.
103003	Test 5	None	
106005	Test 6	E105 DATA IS XXXXXX EXP YYYYYY (UART RCVE # STOP, ZZZ PARITY, # BITS PER CHAR)	The interface is in receive mode. Test serial data is presented to the UART. This data contains all combinations of data, parity, character length and number of stop bits. When no teleprinter is available the A-register contains the actual data and the B-register holds the expected data. The operator presses RUN and a second halt occurs (103005) with the A-register holding the WORD 3 Command used to select the frame parameters.
103005	Test 6	None	
106006	Test 6	E106 PARITY	During a receive operation a parity error has occurred.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106007	Test 6	E107 STATUS IS XXXXXX EXP YYYYYY (BREAK FLAG)	A receive operation is started and the serial data in line is placed in the mark state and held there for sufficient time for the BREAK Flag to set. This Flag is expected in the status word.
106010	Test 6	E110 FLAG NOT SET - BREAK	The interface should set its Flag FF because the BREAK Flag is set.
106011	Test 6	E111 STATUS IS XXXXXX EXP YYYYYY (BREAK RESET)	A WORD 4 Command is given with the Clear BREAK Flag bit set. The status word is then examined for the reset BREAK Flag.
106012	Test 6	E112 STATUS IS XXXXXX EXP YYYYYY (ECHO)	The operation of the ECHO is tested. A receive operation is set up with ECHO enabled. Serial data is presented and the results monitored.
106013	Test 7	E113 BAUD RATE SLOW (XXXX)	A transmit operation is performed and timed. The duration of the transmitted buffer is in excess of 4% of the allowable time. The A-register contains the WORD 4 Command used to select the baud rate.
106014	Test 7	E114 BAUD RATE FAST (XXXX)	Same as E135 except rate is fast. The duration was insufficient. The A-register contains the WORD 4 Command used to select the baud rate.
106015	Test 10	E115 STATUS IS XXXXXX EXP YYYYYY (OVER-RUN)	A receive operation is set up and data is supplied to the interface. The UART is allowed to fill. With excess data presented to the interface, the OVPEFLG is set. The OVPEFLG is expected to be present in the status word.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
106016	Test 10	E116 FLAG NOT SET - OVPEFLG	The interface Flag FF should become set because the OVPEFLG is set.
10o017	Test 10	E117 STATUS IS XXXXXX EXP YYYYYY (OVPEFLG RESET)	A WORD 5 Command is used to reset the OVPEFLG. The status word should indicate the reset condition.
106020	Test 10	E120 NO PARITY ERROR (XXXXXX)	A receive operation is set up and data with incorrect parity is supplied to the interface. The OVPEFLG should become set. The status word is examined for this condition.
10o021	Test 10	E121 OVPELFG NOT RESET	A WORD 5 Command is used to reset the OVPEFLG. A check of the interface status word is then made.
106022	Test 11	E122 FLAG SET - BFFLG (DCPC=1)	Buffer Flags are prevented from setting the interface Flag because DCPC is enabled.
106023	Test 11	E123 FLAG SET - DEVINT, SRQ	A data request is generated. The DCPC is enabled and the Service Request (SRQ) becomes set. Conditions are then created to produce a Device Interrupt. This DEVINT is now prevented from setting the interface Flag FF by the set state of the SRQ FF.
106024	Test 11	E124 FLAG NOT SET-AFTER CLF CH (SRQ)	The pending Device Interrupt is now permitted to set the interface Flag FF because the SRQ FF is reset by the CLF instruction.
106025	Test 11	E125 SRQ SET WHILE LOCK = 1	A Master Reset Command is used to set the LOCK FF. A data request is then generated which is now prevented from setting the SRQ FF by the LOCK.

Table 4-2. Error Information Messages and Halt Codes (Cont.)

HALT CODE	SECTION	MESSAGE	COMMENTS
None	Test 11	H126 DCPC DATA TRANSFER OMITTED-NO DCPC	The configuration of the system does not include a DCPC. There can be no data transfer using DCPC.
106027	Test 11	E127 DATA IS XXXXXX EXP YYYYYY (DCPC TRANSMIT)	A typical data transmit operation is performed using the DCPC to handle the data from memory.
106030	Test 11	E130 STATUS IS XXXXXX EXP YYYYYY (DCPC TEST)	After completing a data transfer using the DCPC the status of the interface is examined and an abnormal response was encountered.
106031	Test 11	E131 DATA IS XXXXXX EXP YYYYYY (DCPC RECEIVE)	A typical data receive operation is performed using the DCPC to transfer data into the memory.
106032	Test 11	E132 DCPC ABEND	After the completion of a DCPC transfer the residual character count in the DCPC should be zero.
106077	Test Control	None	Halt stored in locations 2 through 77 to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot number which interrupted. Diagnostic may be partially destroyed and have to be reloaded if it was caused by a CPU failure; the problem should be corrected before proceeding.

4-13. DEFINITION OF TERMS

ABEND - Abnormal End

BA - Transmit Data
BB - Receive Data
BEFLG - Buffer Empty Flag
BFFLG - Buffer Full Flag

CA - Request To Send (RQS)
CB - Clear To Send (CLS)
CBE - Clear Buffer Empty Status Flag (WORD 5+CBE)
CBF - Clear Buffer Full Status Flag (WORD 5+CBF)
CC - Data Set Ready (DSR)
CD - Data Terminal Ready (DTR)
CE - Ring Indicator (RNG)
CF - Receive Line Signal (RLS)
CHAR CTR - Character Counter

DCPC - Dual Channel Port Controller
DEVINT - Device Interrupt

EN - Enable (WORD 1 Command)

INC - Increment (INC CHAR CTR)

MR - Master Reset (BIT 15 of WORD X Command)

OVPEFLG - Over-run / Parity Error Flag

RCVE - Receive Mode (WORD 4+NOT XMIT)
REF - Reference (Reference WORD 2 Command)

SBA - Secondary Transmit Data
SBB - Secondary Receive Data
SCA - Secondary Request To Send (SRQS)
SCF - Secondary Receive Line Signal (SRLS)
SRQ - Service Request (DCPC)

UART - Universal Asynchronous Receiver/Transmitter

WORD Ø - Transmit Data Word
WORD 1 - Enable Device Status Interrupt Word
WORD 2 - Device Status Reference Word
WORD 3 - Character Frame Control Word
WORD 4 - Interface Control Word
WORD 5 - Interrupt Status Reset Word
WORD 6 - Reserved
WORD 7 - Reserved

XMIT - Transmit Mode (WORD 4+XMIT)

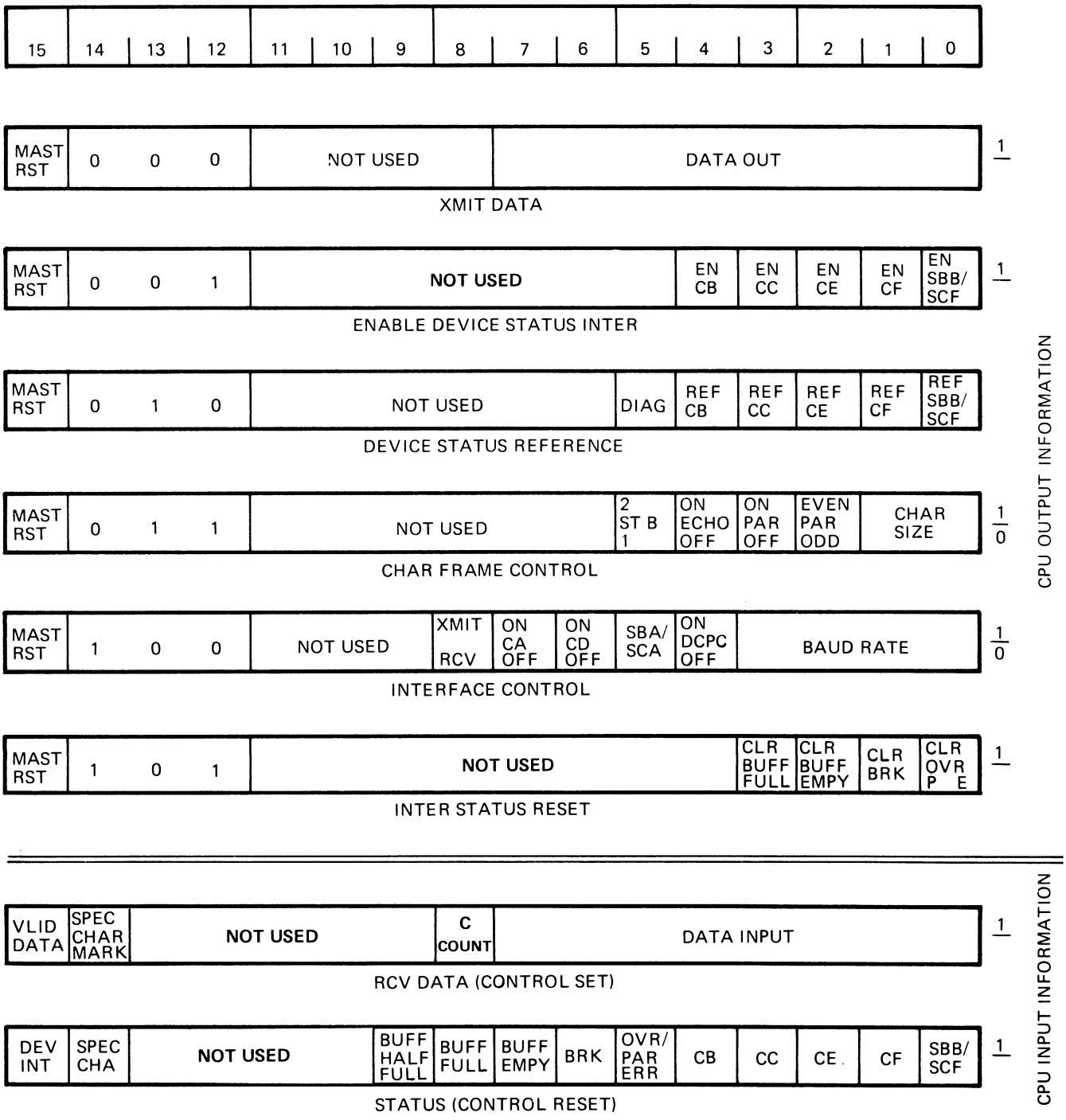

Figure 4-1. Command, Status and Data Formats

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